

REMARKS

Claims 1-13, 16-23 and 25-27 are currently active.

Claims 14, 15 and 24 have been cancelled.

Claim 27 has been added. Antecedent support for Claim 27 is found in Claims 1, 2, 4, 5 and 13.

The Examiner has objected to Claims 11 and 12 to the spelling of comparator. The spelling has been corrected.

The Examiner has rejected Claims 14 and 24 under 35 U.S.C. 112. Claims 14 and 24 have been cancelled.

The Examiner has rejected Claim 15 under 35 U.S.C. 112. Claim 15 has been canceled.

The Examiner has rejected claims 1-9 as being unpatentable over Urbansky in view of Goto. Applicants respectfully traverse this rejection.

Referring to Urbansky, the Examiner admits in section 4 of the Office Action that Urbansky teaches a single source and a first filter for the removal of jitter and wander. The Examiner further states that Urbansky does not explicitly teach a second filter. However, the Examiner writes that Urbansky states there may be a requirement for such a filter and cites page 535, paragraph below figure 1 for this support in Urbansky.

First, Urbansky fails to teach or suggest there be a first filter to remove jitter and a second filter to remove wander, as found in Claim 1 of applicants. Secondly, a review of page 535, paragraph below figure 1 of Urbansky, it simply states that the inherent jitter of such a fractional-N divider corresponds to the reference clock period. It can be reduced by a subsequent PLL. If the frequency range of the jitter spectrum is sufficiently high, analog PLLs with high cut-off frequency and simple oscillators may be employed. The fractional-N divider may be included in the feed forward path for the feedback loop of the jitter suppression. Applicants respectfully submit there is no teaching or suggestion of there being a separate first filter from a second filter where one removes jitter and the other removes wander. In fact, wander is not even stated anywhere in the paragraph. A subsequent review of the entire reference of Urbansky fails to teach or suggest the same. Accordingly, it is respectfully submitted that the statement by the Examiner that Urbansky does teach that there may be a requirement for such a filter, is not present.

It is further submitted and stressed that Urbansky actually teaches away from the claimed invention of applicants because Urbansky teaches for the first filter to remove both jitter and wander, while applicants' claimed invention specifically teaches to have a first filter remove jitter and a separate second filter to remove wander.

Referring to Goto, the Examiner cites Goto because Goto teaches the need for a first loop with high enough bandwidth and gain to pull-in signals quickly to accommodate the jitter and rapid phase transients, and a second loop with low enough bandwidth and gain to maintain clock stability in holdover mode (sought to accommodate wander and meet MTIE requirements, column 1, lines 46-64). It must be stressed that Goto also does not teach or suggest a first filter for removing jitter and a second filter that is separate and apart from the first filter, for removing wander.

Referring to column 1, lines 46-64 of Goto, that the Examiner cites, it is the summary of the invention section which is very broad and ambiguous language. Lines 46-64 specifically state a PLL circuit for producing an error signal representative of a difference between the phase of an input frequency signal and the phase of the output frequency of the VCO, adding a voltage proportional to the error signal and a voltage proportional to the times integral of the error signal to thereby input a sum voltage, and controlling the oscillation frequency of the VCO with the sum voltage by feedback control, the voltage proportional to

the time integral of the error signal as the sum of the output voltage of the first integrator and the output voltage of a second integrator. The feedback loop including the first integrator is provided with a loop gain great enough to reduce the pull-in time. The feedback loop including the second integrator is provided with a loop being small enough to hold over an integrated voltage corresponding to a mean value of differences between the frequencies of the input frequency signal and the self-running frequency of the VCO appeared over relatively long period. As is clear, this paragraph does not even mention jitter or wander, and is a very general statement which does not give one skilled in the art any basis in terms of how to implement such concepts in the context of the architecture taught by Urbansky in regard to a first filter and a second filter as found in Claim 1 of applicants.

In addition, there must be some teaching in the references themselves to combine the specific teachings the Examiner has relied upon to arrive applicants' invention of Claim 1, and there is none. It is respectfully submitted by applicants that this language is so broad it can be interpreted to be anything, yet a careful review of it suggests that the Examiner is reading the limitations of Claim 1 of applicants into this language, where the limitations are not there. Accordingly, Claim 1 is patentable over Urbansky in view of Goto.

Claims 2-9 are dependent to parent Claim 1 and are patentable for the reasons Claim 1 is patentable.

The Examiner has objected to Claims 10-13.

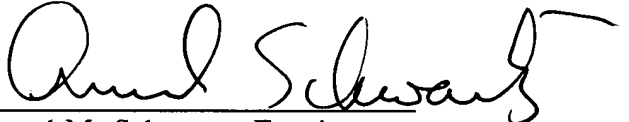
The Examiner has rejected Claims 16-18 as being unpatentable over Urbansky in view of Goto. For the reasons explained above in regard to Claim 1, Claim 16 is patentable over Urbansky in view of Goto. Claims 17 and 18 are dependent to parent Claim 16 and are patentable for the reasons Claim 16 is patentable.

The Examiner has objected to Claims 19-23.

In view of the foregoing amendments and remarks, it is respectfully requested that the outstanding rejections and objections to this application be reconsidered and withdrawn, and Claims 1-13, 16-23 and 25-27, now in this application be allowed.

Respectfully submitted,

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